UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,872	04/20/2004	Kenneth C. Creta	P18867	5618

59796 7590 03/04/2009

INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
UNELUS, ERNEST	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
03/04/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,872	CRETA ET AL.	
	Examiner	Art Unit	
	ERNEST UNELUS	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 21-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/09/09 has been entered.

The rejection(s) of claim(s) 1-36 under Grun (US pat. 6,629,166) have been fully considered and is not persuasive. However, base on the amendment, the rejection has been withdrawn. Therefore, upon further consideration, a new ground(s) of rejection is made in view of Scarpino (US pat. 6,748,496) and Graham et al. (US pat. 6,233,641).

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

4a. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 31-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation 'the I/O hub' in line 9. There is insufficient antecedent basis for this limitation in the claim. 'I/O hub' was not previously mention. **Claims 32 and 33** depends from claim 31 and therefore inherits the above described deficiency.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

4b. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. **Claims 1-4, 10-15, 21-25, 30, and 34-35,** are rejected under 35 U.S.C. 102(e) as being anticipated by Scarpino (US pat. 6,748,496).

6. As per **claims 1 and 34**, Scarpino discloses "A method comprising:

receiving a plurality of partial data write transactions **(see col. 4, line 65 to col. 5, line 1, which discloses, "When the bridge 80 see data that belongs to a data burst, the bridge will collect the write transactions from either processor 60 or processor 66 into a write combining buffer 52")**, each of the plurality of partial data write transactions including a write combinable attribute to indicate they are write combinable partial data write transactions **(see col. 5, lines 5-12, which discloses the attribute, the 'specific condition')**;

combining partial data associated with the plurality of partial data write transactions in a buffer of an input/output (I/O) hub **(the bridge)** to form write combined data in response to each of the plurality of partial data write transactions including the write combinable attribute to indicate they are being write combinable partial data write transactions **(see col. 5, lines 1-12)**; and

flushing the write combined data associated with the plurality of write transactions to an I/0 device **(see col. 5, lines 13-16 and col. 6, lines 1-6, which discloses flushing data to a graphics controller)**.

7. As per **claims 2, 13, 22, and 35**, Scarpino discloses "The method of claim 1," **[See rejection to claim 1 above]**, wherein flushing the data to the I/O device includes: determining whether a flush signal has been received from a processor **(see col. 6, lines 1-6)**; and flushing the data if the flush signal has been received **(col. 6, lines 1-6)**, the protocol including an signaling protocol **(col. 6, lines 1-6)**.

8. As per **claims 3 and 14**, Scarpino discloses "including sending a write completion signal to the processor for each of the plurality of partial data write transactions before the data is flushed to the I/O device, wherein each write completion signal is to verifying buffering of a corresponding partial data write transaction of the plurality of partial write transactions **(see col. 3, lines 25-45 and col. 6, lines 1-6)**.

9. As per **claims 4 and 15**, Scarpino further discloses "including sending a-flush completion signal to the processor after the data is flushed to the I/O device **(see col. 3, lines 25-45 and col. 6, lines 1-6)**.

10. As per **claim 10**, Scarpino discloses "wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device **(see fig. 2 and col. 6, lines 1-6)**.

11. As per **claim 11**, Scarpino discloses "wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands **(see col. 5, lines 1-12)**.

12. As per **claim 12**, Scarpino discloses an input/output (I/0) hub comprising:

receiving logic to receive a first write transaction and a second write transaction from a processor **(see fig. 2 and col. 4, line 65 to col. 5, line 1, which discloses, "When the bridge 80 see data that belongs to a data burst, the bridge will collect the write transactions from**

either processor 60 or processor 66 into a write combining buffer 52"), the first and the second write transactions to reference partial data of a cache line within the processor, wherein the first and second write transactions include a write combinable attribute to indicate the first and the second partial write transactions as write combinable **(see col. 5, lines 5-12, which discloses the attribute, the 'specific condition')**, combining logic coupled to the receiving logic to combine the partial data of the cache line referenced by the first and second write transactions as write combined data in response to the first and second write transactions including the write combinable attribute to indicate they are write combinable **(see col. 5, lines 1-12)**; and

flushing logic coupled to the combining logic to flush the write combined data to an I/0 device in response to a protocol event **(see col. 5, lines 13-16 and col. 6, lines 1-6, which discloses flushing data to a graphics controller)**.

13. As per **claim 21**, Scarpino discloses a system comprising:

an input/output (I/O) device **(graphics controller 90)**;

a processor to associate a write combinable attribute with a plurality of write transactions to identify them as write combinable and to transmit the plurality of write transactions, wherein each of the write transactions are to be associated with partial data **(see col. 4, line 65 to col. 5, line 1, which discloses, "When the bridge 80 see data that belongs to a data burst, the bridge will collect the write transactions from either processor 60 or processor 66 into a write combining buffer 52")**; and

an I/O hub **(the bridge)** coupled to the I/O device s and the processor, the I/O hub having a write combining module to receive the plurality of write transactions from the processor, to

combine the partial data associated with the plurality of write transactions to form a write combined data set in response to the plurality of write transactions being associated with the write combinable attribute to identify them as write combinable transactions **(see col. 5, lines 5-12, which discloses the attribute, the 'specific condition')**, and to transmit the write combined data set to the I/O device in response to a protocol event associated with the processor **(see col. 5, lines 1-16).**

14. As per **claim 23**, Scarpino discloses wherein the processor is to generate the flush signal in response to a flushing event occurred and a write combine history indicates that one or more combinable write transactions have been issued by the processor **(see col. 5, lines 13-16 and col. 6, lines 1-6).**

15. As per **claims 24 and 25**, Scarpino discloses wherein the write combine history is to track combinable write transactions for a particular processor thread and an I/O hub **(see col. 5, lines 13-16 and col. 6, lines 1-6)**.

16. As per **claim 30**, Scarpino discloses "including a point-to-point network interconnect coupled to the processor and the I/O hub, the network interconnect having a layered communication protocol **(see fig. 2 and col. 4, lines 55-61)**.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. **Claims 5-9, 16-19, 26-29, 31-33, and 36**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Scarpino (US pat. 6,748,496) in view of Graham et al. (US pat. 6,233,641).

19. As per **claim 5**, Scarpino discloses "The method of claim 2," **[See rejection to claim 2 above]**, including wherein flushing the data if the flush signal has been received further includes: tagging the buffer with a first source identifier associated with one or more of the write transactions; detecting a second source identifier associated with the flushing signal **(see col. 5, lines 5-12)**, but fails to disclose expressly comparing the second source identifier to the first source identifier ; and flushing the data to the I/O device if the second source identifier matches the first source identifier

Graham discloses determining comparing the second source identifier to the first source identifier; and flushing the data to the I/O device if the second source identifier matches the first source identifier **(see col. 6, lines 40-50 and col. 7, lines 6-15).**

Scarpino (US pat. 6,748,496) and Graham et al. (US pat. 6,233,641) are analogous art because they are from the same field of endeavor of a processor using an I/O hub to transmit data to an I/O device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a method and apparatus for providing cacheable data to a peripheral device as described by Scarpino and a routing circuit that functions as a bridge between the primary bus and each of the first and second secondary busses, respectively, by associating each secondary bus with an address range, and forwarding a command received from the primary bus to a secondary bus mapped to an address range including the address of the command as taught by Graham.

The motivation for doing so would have been because Graham teaches that "**the routing circuit directly routes to the second secondary bus, a command received from the first secondary bus addressed for the second secondary bus, without use of the primary bus. As a result, traffic and latency on the primary bus is reduced and efficiency is increased.**" **(see col. 2, lines 38-44).**

Therefore, it would have been obvious to combine Graham et al. (US pat. 6,233,641) with Scarpino (US pat. 6,748,496) for the benefit of creating the method to obtain the invention as specified in claim 5.

20. As per **claims 6 and 19**, Graham further discloses "including repeating the comparing for a plurality of buffers, each buffer corresponding to an I/O port **(see fig. 2B of Graham)**.

21. As per **claims 7, 16, and 36**, Scarpino discloses "The method of claim 1," **[See rejection to claim 1 above]**, including flushing a data to an I/O device but fails to disclose expressly

determining whether a latency condition exists; and flushing the data according to a timing protocol in response to the latency condition existing.

Graham discloses determining whether a latency condition exists **(see col. 6, lines 40-50)**; and flushing the data according to a timing protocol in response to the latency condition existing **(see col. 6, lines 40-60)**.

Scarpino (US pat. 6,748,496) and Graham et al. (US pat. 6,233,641) are analogous art because they are from the same field of endeavor of a processor using an I/O hub to transmit data to an I/O device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a method and apparatus for providing cacheable data to a peripheral device as described by Scarpino and a routing circuit that functions as a bridge between the primary bus and each of the first and second secondary busses, respectively, by associating each secondary bus with an address range, and forwarding a command received from the primary bus to a secondary bus mapped to an address range including the address of the command as taught by Graham.

The motivation for doing so would have been because Graham teaches that " **the routing circuit directly routes to the second secondary bus, a command received from the first secondary bus addressed for the second secondary bus, without use of the primary bus. As a result, traffic and latency on the primary bus is reduced and efficiency is increased." (see col. 2, lines 38-44).**

Therefore, it would have been obvious to combine Graham et al. (US pat. 6,233,641) with Scarpino (US pat. 6,748,496) for the benefit of creating the method to obtain the invention as specified in claims 7, 16 and 36.

22. As per **claims 8 and 17**, the combination of Scarpino and Graham discloses "The method of claim 7," **[See rejection to claim 7 above]**, Scarpino and Graham further disclose including sending a write completion signal to a processor for each of the partial write transactions as the data is flushed to the I/O device **(see col. 6, lines 40-50 of Graham)**, each write completion signal verifying flushing of a corresponding write transaction **(see col. 6, lines 1-6 of Scarpino and col. 7, lines 6-15 of Graham)**.

23. As per **claims 9 and 18**, the combination of Scarpino and Graham discloses "The method of claim 7," **[See rejection to claim 7 above]**, Graham further discloses "wherein the latency condition includes a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state **(see col. 6, lines 40-50 of Graham)**.

24. As per **claim 26**, , the combination of Scarpino and Graham discloses wherein the chipset includes a plurality of I/O hubs, the processor to send the flushing signal to each of the plurality of I/O hubs **(see fig. 2A of Graham)**.

25. As per **claim 27**, , the combination of Scarpino and Graham discloses wherein the processor is to verify that one or more combinable write transactions have been sent to each of the plurality of I/O hubs before sending the flushing signal **(see col. 6, lines 40-50 of Graham)**.

26. As per **claim 28**, , the combination of Scarpino and Graham discloses wherein the protocol event includes a latency condition **(see col. 6, lines 40-50 of Graham)**.

27. As per **claim 29**, , the combination of Scarpino and Graham discloses wherein the processor is to instruct the I/O hub to consider each write transaction for write combining based on a page table attribute associated with the write transactions **(see fig. 2B of Graham).**

28. As per **claim 31**, Scarpino discloses "A method comprising:

receiving a plurality of write transactions from a processor **(see col. 4, line 65 to col. 5, line 1, which discloses, "When the bridge 80 see data that belongs to a data burst, the bridge will collect the write transactions from either processor 60 or processor 66 into a write combining buffer 52")**, the plurality of write transactions being destined for an input/output (I/O) device **(graphics controller 90)**; storing data associated with the plurality of write transactions to a buffer **(write combining buffer 52, 54 in drawing)** of the I/O hub **(bridge 80)** in response to the plurality of write transactions being identified as write combinable transactions **(see col. 5, lines 1-12)**; flushing the data to the I/O device if the latency condition exists **(see col. 5, lines 13-16 and col. 6, lines 1-6, which discloses flushing data to a graphics controller)**.

but fails to disclose expressly determining whether a latency condition exists, the latency condition including a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state; and sending a write completion signal to the processor for each of the plurality of write transactions as the data is flushed to the I/O device, each write completion signal verifying flushing of a corresponding write transaction.

Graham discloses determining whether a latency condition exists, the latency condition including a delay in receiving a next combinable write transaction from the processor and an interface to the I/O device being in an idle state; and sending a write completion signal to the processor for each of the plurality of write transactions as the data is flushed to the I/O device, each write completion signal verifying flushing of a corresponding write transaction **(see col. 6, lines 40-50 and col. 7, lines 6-15 of Graham)**.

Scarpino (US pat. 6,748,496) and Graham et al. (US pat. 6,223,641) are analogous art because they are from the same field of endeavor of a processor using an I/O hub to transmit data to an I/O device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a method and apparatus for providing cacheable data to a peripheral device as described by Scarpino and a routing circuit that functions as a bridge between the primary bus and each of the first and second secondary busses, respectively, by associating each secondary bus with an address range, and forwarding a command received from the primary bus to a secondary bus mapped to an address range including the address of the command as taught by Graham.

The motivation for doing so would have been because Graham teaches that " **the routing circuit directly routes to the second secondary bus, a command received from the first secondary bus addressed for the second secondary bus, without use of the primary bus. As a result, traffic and latency on the primary bus is reduced and efficiency is increased." (see col. 2, lines 38-44).**

Therefore, it would have been obvious to combine Graham et al. (US pat. 6,233,641) with Scarpino (US pat. 6,748,496) for the benefit of creating the method to obtain the invention as specified in claim 31.

29. As per **claim 32**, the combination of Scarpino and Graham discloses "The method of claim 31," **[See rejection to claim 31 above]**, Scarpino further discloses "wherein flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device **(see fig. 2)**.

30. As per **claim 33**, the combination of Scarpino and Graham discloses "The method of claim 31," **[See rejection to claim 31 above]**, Scarpino further discloses "wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands **(see col. 3, lines 25-45)**.

RELEVANT ART CITED BY THE EXAMINER

31. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

32. The following reference teaches write transactions on an input/output (I/O) hub according to a protocol between the target and a processor.

U.S. PATENT NUMBER

US 6,553,446

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

33. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

34. Per the instant office action, claims 1-19 and 21-36 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

36. If attempts to reach the above noted Examiner by telephone are unsuccessful,

the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

February 26, 2009
/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

Ernest Unelus
Patent Examiner
Art Unit 2181

/E. U./
Examiner, Art Unit 2181